Maximizing power device yield with in situ trench depth measurement

EXECUTIVE OVERVIEW Many power devices rely on a silicon trench technology for operation. This article discusses the importance of trench depth control, provides examples of various trench etch applications, and evaluates a technique for in situ depth monitoring. Finally, the implications of these techniques on device yield are considered.

Power handling is a pervasive area of the semiconductor industry with power devices present in everyday products such as PCs, PDAs, automobiles, handsets, and white goods. For several types of power semiconductors, significant advantages in device performance can be achieved by the use of a silicon trench technology.

In the case of a trench MOSFET power device, the feedback capacitance, C_{gd}, between the gate and drain regions largely determines the device switching speed [1]. The larger C_{gd} becomes, the longer it takes to switch charge, and the slower the device becomes, leading to intolerable losses for devices designed to operate at high frequency. The gate polysilicon and the drain silicon form the capacitor. Theoretically, the best devices are made when the trench is narrow and extends just beyond the p-n interface.

The ultimate trench width is governed by the photolithographic capabilities of the specific manufacturer and the compatibility with subsequent processing steps. The position of the p-n junction can be accurately controlled during ion implantation. This leaves trench depth control as the major factor involved in minimizing C_{gd}, and it is the most critical parameter to control during the etching of silicon trenches. Other parameters to control include the smoothness of the trench sidewall (which minimizes the gate leakage current), the sidewall profile (for successful filling with polysilicon while avoiding 'key hole' voids), and trench bottom rounding.

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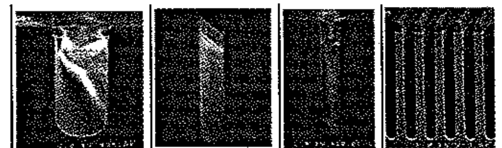
Chemistry and plasma source

Table 1 summarizes various chemistries that may be used for etching trenches in silicon. Aviza uses the SF_6/O_2 approach for trench etching for power devices. This approach relies on balancing etching reactions between F-atoms and the silicon substrate (to form SiF_x by-products) with sidewall passivation due to the interaction of the etched silicon sidewall with oxygen in the plasma (to produce SiO_y). Where required (mainly for deep structures), additional sidewall protection can be achieved by adding CF_4 or SiF_4 into the process gas mix.

Figure 1 shows a broad range of typical silicon trenches that are required for power device production. Each trench is characterized by having a smooth sidewall with a slightly tapered (~89° profile) and a rounded bottom section. The silicon etch rates for these processes are in the range of 2.2–3.6µm/min, delivering throughputs of 20–33wph per inductively coupled plasma (ICP) process module. Within-wafer etch rate uniformities are typically in the range ±1.0–2.5% (max-min/2x mean). Additional details regarding the key process parameters that influence the etch rate uniformity, trench bottom rounding, sidewall angle, and CD loss can be found in a separate article [7].

Table 1. Comparison of approaches for etching silicon trenches

Chemistry	Silicon etch rate	Mask selectivity	Sidewall smoothness	Hardware required
NF_3-based	Low-Medium	High	Good	Standard
Cl_2-based [2, 3]	Low	High	Medium	
SF_6/O_2-based [4]	High	Medium	Good	Standard
SF_6-cryogenic [5]	High	Medium	Good	Requires cryogenic chuck
SF_6/C_4F_8 'Bosch' [6]	High	High	Poor	Requires fast gas switching



Width (µm), aspect ratio	1.0, 2:1	0.5, 4:1	1.5, 4:1	0.6, 8:1
Etch rate (µm/min)	2.2	2.6	3.6	2.7
Wph per chamber	~30	~33	~26	~20

Figure 1. Examples of typical trenches required for production of power devices.

In situ diagnostics

Controlling the trench etch depth is more difficult than for most dry etch applications because for most power devices there is no stop layer at which etching can be terminated using conventional optical emission spectroscopy (OES). Attempting to control the depth simply by adjusting the process time is subject to many possible inconsistencies, such as variations due to chamber condition or loading effects due to mask open area changes from device to device. Typically, only ±4% depth accuracy wafer-to-wafer is achieved with timed etches, and in many cases, this level of control is insufficient for high device yield.

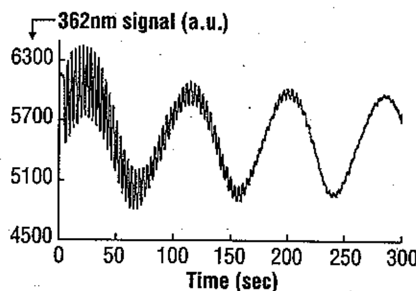


Figure 2. Typical IEPD trace for 15μm deep trench.

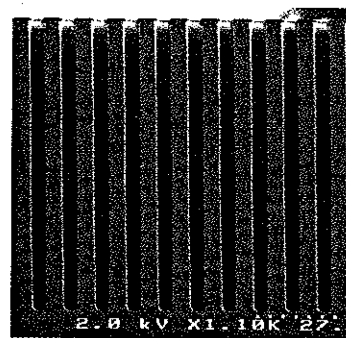


Figure 3. An ~3x 70μm power trench etched using the Bosch process.

To meet the trench depth repeatability levels that are required for robust manufacturing, it is necessary to integrate an analytical tool onto the etch chamber that can directly measure or compute the etch depth in real time. Interferometric endpoint detection (IEPD) represents a method of depth monitoring. The technology is implemented with a 'white' light source, an optical tilt head assembly, and a combined wavelength selection and detection unit. The white light source emits a broadband optical signal that is transmitted via optical fibers to the optical tilt head assembly situated on a central viewport of the ICP chamber.

The process gas is also introduced centrally. The tilt head assembly produces a collimated light beam normal to the wafer surface. Adjustment of the tilt head enables accurate alignment of the beam relative to the wafer. The sampling area on the wafer is typically 15mm in dia. There is no requirement to align the beam relative to the features on the wafer—IEPD effectively samples an average of etched and nonetched areas. Light reflected from the wafer is collected by the same assembly and transmitted by optical fiber to the detector, which measures the light intensity at a preselected wavelength.

A PC captures the oscillating light intensity and uses Fourier analysis to directly calculate the silicon etch rate and trench depth. The analytical units (interferometers) are commercially available (examples include the Verity SP2000 spectral reflectometer and the JY Horiba Digilem white light interferometer).

A typical output signal of optical intensity measured during the etching of a silicon trench is shown in **Fig. 2**. In this case, the trench is 15μm deep. The optimum wavelength that is chosen for a particular trench etch is dependent upon the intensity of the signal compared to the intensity of the plasma itself, the depth of the trench (because the reflection of longer wavelengths from the base of the trench become suppressed with depth), and the transparency of the masking layer.

Figure 2 shows two superimposed oscillation frequencies. One has a period of ~100 seconds and is due to the erosion of the mask layer (in this case, silicon dioxide) and the higher frequency response has a period of ~3 sec and is due to the etching of the silicon trench itself. The ratio of these periods reflects the etch selectivity of silicon relative to the mask, as confirmed by SEM measurement to be ~35:1.

For much shallower trenches, differentiation and smoothing algorithms are used to assist in separating the two oscillations. A Fourier transform of the signal is used to identify the frequency of the silicon trench oscillation, which is converted into a silicon etch rate using the formula:

$$Er_{tr} = \frac{60 f \lambda}{2}$$

where Er_{tr} is the trench etch rate in nm per minute, f is the frequency of oscillation in Hz, and λ is the wavelength in nm.

Figure 2 also shows a limitation of the IEPD approach. The interference fringes for the etching of the trench reduce in amplitude as the trench deepens. The trench bottom basically becomes less efficient at reflecting the incident light back to the detector—a situation exacerbated by the preferred rounding of the bottom section. This limits the depth to which the trench can be directly monitored to ~10μm. However, for deeper trenches it is adequate to monitor the depth for the initial 10μm and then compute the end-point time for the full

The market for power devices

Maximal critical dimension: 4μm design rule smart power; 2μm design rule smart power; 1μm design rule smart power; 0.5μm design rule smart power; 0.35μm design rule smart power

Wafer thickness: Thin wafer technology (300μm); Thin wafer technology (200μm); Ultrathin wafer technology (85μm); Ultrathin wafer technology (65μm)

Deep etch: Deep trench isolation; Super junction CoolMOS; Trench gate technology; MDMESH; Deep trench super junction; Deep etch on new materials (SiC, diamond)

Materials: SOI wafers; SiC (Schottky); Partial SOI wafers; SiC devices (MOSFET); Diamond device (FED)

1980 1990 2000 2010 2020

According to a report from market research firm Yole Développement (PowerD'06: Analysis of advanced technologies and related markets for power devices), the power devices market was valued at $22.6B in 2005 and is set to reach $29.5B by 2008. Wafer consumption in 2004 for all power devices was ~13.2M (6-in. wafer equivalents) and currently represents ~10% of the total consumed by the semiconductor IC industry. The most common discrete components are power MOSFETs accounting for ~35% of the discretes market. The timelines above, courtesy of Yole Développement, show the emerging technologies roadmap for power device production. ■

process by assuming an etch time for the latter stages.

It turns out that trenches deeper than ~15μm are difficult to etch with the SF_6/O_2 approach due to breakdown of the passivated sidewall near the top of the trench—this can be the case even when additional passivation gases (such as CF_4) are introduced. For this reason, deep trenches for power devices are also starting to be etched using the Bosch gas-switched approach. **Figure 3** is an example of etching to a depth of 70μm using this technique. Scalloping of the sidewall (a natural consequence of the Bosch approach) may be minimized by increasing the switch times and limiting the net etch rate. In any case, scalloping tends to be restricted to the upper portions of high aspect trenches like these (<5μm depth, in this case).

Table 2. Trench depth control by IEPD

Targeted etch depth (μm)	Measured etch depth, center wafer (μm)	Difference (μm)
1.55	1.53	-0.02
1.25	1.29	0.04
1.85	1.85	0.00
1.40	1.41	0.01
1.70	1.71	0.01

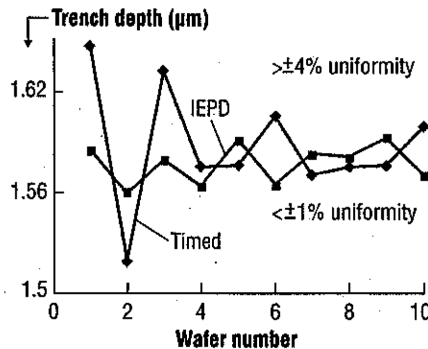


Figure 4. Comparison of trench depths by AFM for timed and IEPD monitored wafers.

Trench depth repeatability

IEPD allows the silicon trench etch to be terminated at a preprogrammed depth. The process time is allowed to 'float' to the point at which the required depth is achieved and provides for the following: 1) automatic compensation for etch rate variations introduced by the process chamber condition; 2) automatic compensation for etch rate variations introduced by the wafer condition; 3) minimizing the number of sacrificial test wafers normally required in production; 4) minimizing development effort on new products; and 5) improving the trench depth repeatability

The ability of IEPD to actively control etch depth is shown in **Table 2**. Good correlation is achieved between the targeted and the actual etch depths. There were no process changes for these wafers—only changes to the IEPD depth set-point. All depth measurements were by ex situ atomic force microscopy (AFM).

Figure 4 shows trench depths measured by AFM across 10 wafers processed consecutively. The data for the timed etches shows a marked instability, particularly for the first few wafers processed, and results in a wafer-to-wafer uniformity of >±4% (max-min/2x mean). In contrast, the trenches monitored by IEPD have a more consistent trench depth even across the first few wafers and return a wafer-to-wafer uniformity of <±1%. The variability of the timed etches could be due to many factors including gradual conditioning of the plasma chamber, changes to the temperature of chamber furniture, or effects introduced by variability on wafer. In a sense, the root cause does not matter because the interferometer is able to compensate for these variations via the 'floating' etch time.

Figure 5 shows endpoint times measured during the etching of multiple wafers and batches. **Figure 5a** is for wafers etched to a target depth of 1.5μm. The actual depths of these trenches have not been measured. However, the spread in endpoint times—the process times that correspond to a fixed trench depth of 1.5μm as given by the IEPD system—can be used to assess the variation in depths that would result if the etches were simply timed.

Batch #1 produces a uniformity of endpoint times of ±3.2% (max-min/2x mean). When all batches from Fig. 5a are included, the uniformity is ±4.0%. These numbers are fairly typical of most timed etches. High-etch rate processes like these are more likely to suffer wafer-to-wafer variability due to hardware limitations on the system (such as the finite times taken for RF matching and the ability to switch off RF supplies at precise times).

Generally speaking, there is a trend toward shorter endpoint times as each cassette of wafers is processed, presumably due to gradual conditioning effects of the process chamber and/or temperature changes as each wafer is processed. The fact that the data for the four batches are roughly superimposed signifies that there is no memory effect of the conditioning or temperature change over the time taken to remove one batch of wafers and load another (typically 5–6 min. in this case).

Figure 5b is for wafers etched to a target depth of 5.5μm. Similar trends are seen as wafers are processed, but in this case, there is a more significant first wafer effect. The uniformity for the 11 wafers of Batch #1 is ±2.0%

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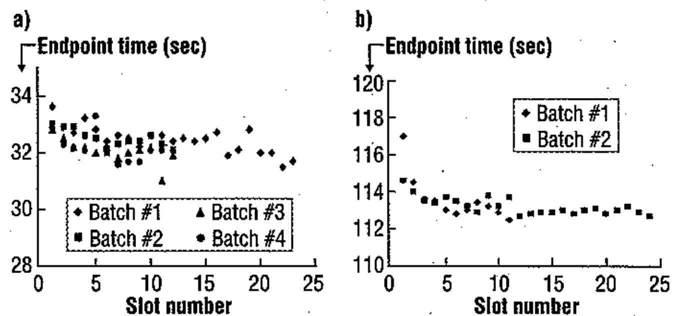

Figure 5. Variation in endpoint times for multiple wafers and batches for: a) 1.5μm deep trenches, and b) 5.5μm deep trenches.

Table 3. IEPD results on multiple power product types

Product type	# of wafers	Process	IEPD end-point setting	Target depth (μm)	Average wafer center depth (μm)	Center depth variation, 1σ (μm)
#1	10					
#2	10					
#3	10	Constant	Constant	1.550	1.543	0.011 (0.7%)
#4	10					
#5	10					

All of the examples in Fig. 4 are well-matched between references and mask images. Therefore, we can expect no false defect detections, while defects that are detected will be stable during the sensitivity evaluation.

Detectability and printability of programmed defects. Figure 5a shows the detectability and printability summary of five inspection runs on Qz bump defects. **Figure 5b** illustrates the summary for Cr residue defects. The graph shows the results for all defect categories on all four basic design patterns indicated at the top of the column. The defect design size is indicated in the left-most column. The colored box in each cell denotes 100% detection and the listed value indicates the percentage detection out of the five inspection runs. Red horizontal lines indicate the boundary for >10% CD change as confirmed by AIMS analysis, and blue dotted lines indicate where defects would cause >5% CD change simulated at the wafer scale.

The results described above imply that all 120° Qz bumps or Cr residue defects that cause 10% CD error as defined by AIMS analysis were detected by the KLA576 two-layer database transmitted light inspection. While the detection capability of edge-type Qz defects for categories #2 and #3 is relatively easy compared to that for categories #1 or #4, it can be said that the detectability is too high on these categories and the same thing is confirmed on all categories of Cr residue defects. Further development of defect disposition methodology is expected for these defect categories.

Conclusion

We have successfully inspected a production-like 65nm node CPL logic gate pattern that has a full tri-tone design. It was confirmed that good defect detectability is possible using KLA-Tencor's two-layer database inspection technology. The data preparation system successfully handled two-layer databases, and the rendering system created a tri-tone database image. Light calibration and pre-swath calibration produced a processed reference image that is well-matched to the mask image at the shifter region and the chrome SRAF. The TeraScan two-layer database inspection detection capability of 10% CD change on the wafer caused by defects was confirmed by AIMS analysis with a very low false defect detection rate. ■

Acknowledgments

The author would like to thank Cikashi Ito of KLA-Tencor/Japan and John Miller and Larry Zurbrick of KLA-Tencor for their technical support in evaluating the analysis of inspection results. The author also thanks Kouichirou Kojima, Hidemichi Imai, Hiroyuki Hashimoto, and Shiho Sasaki of DNP for their technical support of the CPL mask fabrication, inspection data analysis, and AIMS data analysis.

CPL is a trademark of ASML MaskTools. AIMS is a trademark of Carl Zeiss. AR8 is a product name of HOYA.

Reference

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Fast development on varying product types

Table 3 summarizes the results of using IEPD on five different power product types from one customer that have different exposed areas, trench sizes, and device layouts. The mask type and thickness were held constant, as were the process conditions and the IEPD settings.

Timed etches are incapable of delivering the depth repeatability required for robust power device manufacturing because changing chamber conditions cause process time variability. To meet trench depth repeatability requirements, analytical tools need to be integrated onto the etch chamber that can directly measure or compute the etch depth in real time. Test results show that interferometric endpoint detection is capable of fast trench etch development without extensive processing of test wafers.

This data was gathered over a one-week period that was interspersed with routine production. Trench depths were measured by AFM.

The tight distribution of center depths across the 50 wafers and five product types demonstrates that IEPD is capable of fast trench etch development without the need for extensive processing of test wafers.

Conclusion

Silicon trench etching is a critical step in the manufacture of a range of power devices. Timed etches are incapable of delivering the required depth repeatability due to a range of factors such as chamber conditions varying the process time required for every wafer. IEPD eliminates etch time as a process variable, and is capable of delivering the trench depth control required to maximize device yield and minimize costs. ■

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